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REVIEW OF CAPACITIVE DAC BASED SUCCESSIVE APPROXIMATION ANALOG TO DIGITAL CONVERTER

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ABSTRACT

Analog to Digital converters are essential between analog and digital circuits. It is one of the most important building blocks in sensor node which digitize the analog environmental information we live in. Many different kinds of analog to digital converter architectures are available such as Flash Type, Integrating type, Pipelined, Time Interleaved and Successive Approximation type. Successive Approximation Register ADC has always been considered for optimizing its Parameters like Speed, Static and Dynamic Error, Power Consumption by a designing a new switching method of the capacitive structure of Digital Analog Converter which is the heart of it. This paper presents the review of existing SAR architectures.

Keywords: CDAC, SAR ADC, ENOB, INL, DNL

I. INTRODUCTION

Digital audio and video have created the need for cost-effective data converters that will achieve higher speed and resolution. The needs required by digital signal Processors continually challenge analog designers to improve and develop new ADC and DAC architectures. High speed and medium resolution analog to digital converters (ADCs) find a wide range of applications in many different areas, such as high speed wireless communication systems. In these applications, low power and small area ADCs requiring conversion rates higher than 60 MS/s and resolution in the range of 7-9 bits are considered an important building block. Among many ADC architectures, Successive Approximation Register ADCs have proven to be very efficient for meeting the above requirement of high speed. SAR is most attractive architecture due to its structural simplicity. It consists of a Digital to Analog converter, Successive Approximation Logic and a Comparator. Analog to Digital conversion relies basically on the performance of binary weighted capacitive DAC array that subtracts the reference voltage from the input signal. It has become popular as an alternative to the pipelined ADCs for battery powered mobile applications. Analog to Digital converters are key design blocks in modern microelectronic digital communication systems. With the fast advancement of CMOS (Complementary Metal Oxide Semiconductor) fabrication technology, more and more signal processing functions are implemented in digital domain for a lower cost, lower power consumption and higher speed. This has generated a low power low voltage ADCs that can be realized in a mainstream

submicron CMOS technology. Many different kinds of analog to digital converter architectures are available such as Flash Type, Integrating type, Pipelined, Time Interleaved and Successive Approximation type.

Flash analog-to-digital converters, also known as Parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Flash ADCs are ideal for applications requiring very large bandwidth, but they consume more power than other ADC architectures and are generally limited to 8-bit resolution. The pipelined analog-to-digital converter (ADC) has become the most popular ADC architecture for sampling rates from a few mega samples per second (Msps) up to 100Msps+ [1]. Resolutions range from eight bits at the faster sample rates up to 16 bits at the lower rates. Each stage performs an operation on the signal, provides the output for the following sampler, and, once the sampler has acquired the data, begins the same operation on the next signal. Different stages process different samples concurrently. Throughput rate depends on only the speed of each stage and the acquisition time of the next sampler. Their area and power dissipation grow almost linearly with the number of bits. A time-interleaved ADC involves more than just placing a few non interleaved ADCs in parallel, since the requirements for a non-interleaved Track and Hold circuit and ADC differ from that of a time-interleaved Track and Hold and sub-ADC: aspects like offset, gain error and absolute timing, which are usually not an issue for a general purpose non-interleaved Track and Hold and ADC, are important for a time-interleaved architecture.

SAR is most attractive architecture due to its structural simplicity. It consists of a Digital to Analog converter, Successive Approximation Logic and a Comparator. Analog to Digital conversion relies basically on the performance of binary weighted capacitive DAC array that subtracts the reference voltage from the input signal and there are still ongoing efforts to further optimize the SAR architectures. It has become popular as an alternative to the pipelined ADCs for battery powered mobile applications.

Specifications of Digital to Analog Converter are Accuracy, static errors i.e. offset and gain errors, Dynamic errors i.e. full scale error and linearity error that includes Differential Non Linearity (DNL) and Integral Non Linearity (INL), Monotonocity, Resolution (Step Size), settling Time [2]. Specifications of Analog to Digital converter are Resolution, Quantization error, Differential Non Linearity, Integral Non Linearity, Conversion Time, Input Voltage Range.

II. REVIEW

The successive approximation converter basically performs a binary search through all possible quantization levels before converging on the final digital answer. An N-bit register controls the timing of the conversion where N is the resolution of the ADC as shown in Figure 1 [3]. Input analog voltage (V_{IN}) is sampled and compared to the output of the DAC. The comparator output controls the direction of the binary search, and the output of the successive Approximation Register is the actual digital conversion.

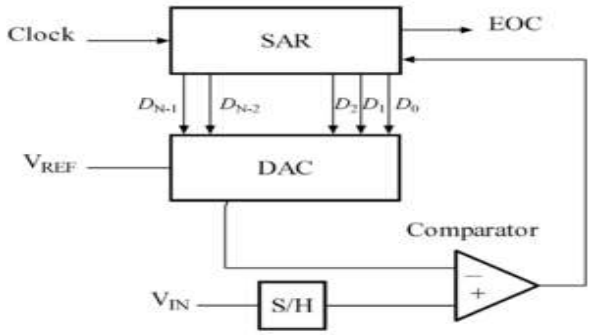

Figure 1: SAR ADC

SAR conversion basically lies on the performance of a capacitive DAC that subtracts the reference voltage from the input signal. Capacitor mismatches of the DAC array and parasitic of the split DAC affect the conversion accuracy [4]. Non-idealities like parasitic and nonlinearity whose effect depends on the structure and switching approach of the DAC are more significant. A binary weighted capacitive DAC is used in SAR ADCs. However, the capacitance of the DAC array increases exponentially with the resolution [5], which imposes larger consumption of the switching energy, area and settling time. In addition control logic becomes complicated due to the increased numbers of capacitors and switches. A valuable substitute is the split capacitance DAC which has recently been considered for medium resolution. Its key limitation lies in the parasitic capacitors that destroy the desired binary ratio of the capacitive DAC array, thus degrading the conversion linearity. Various switching methods have been designed for the split DAC structure.

In 2008, Yan Zhu et. al proposed a 1.2V, 8 bit, 180 MS/s a split capacitor array to optimize the power efficiency and speed of SAR ADC's. The proposed series combination of the split capacitor array resulted in smaller values of capacitor ratios and a more power-efficient charge recycling approach in DAC capacitor array [6]. It shows a SFDR and SNDR of 58 dB and 48 dB respectively for a 76 MHz input with a total power consumption of 14mw. In 2009, Chung-cheng et. al proposed 0.92mw 10-bit 50 MS/s SAR ADC using a set and down switching method to save the power consumption in switching procedure without splitting or adding any capacitors and used a smaller area. This avoided the more complicated control logic due to the increased capacitors and switches used in the other switching methods [7]. When the input frequency is up to 50 MHZ, measured peak DNL and INL of this ADC were +0.88/-1.00 LSB and +2.20/-2.09 LSB and it showed a SFDR and SNDR of 60.09 dB and 50.94 dB respectively. In 2009 Zhieheng Cao et. al designed a 32mw 1.25 GS/s 6bit 2b/step SAR ADC by time interleaving two SAR ADCs with 2.5 GHZ internal clock frequency [8]. Yan Zhu et. al proposed a 10 bit 100-MS/s VCM based split DAC structure to achieve the high speed and low power operation. This design obtained a medium resolution and high conversion speed by avoiding the reference generator which is the large cause of power consumption and directly using the supply voltage and by using a common mode based charge recovery switching method that saves the switching energy during the SA conversion and improves conversion linearity [9]. Peak DNL and INL of this ADC were +0.79/-0.27 LSB and +0.86/-0.78 LSB and it showed a SNDR of 56.6dB and SFDR of 50.71dB respectively.

In 2010, Young Kyun Cho et. al proposed 9-bit 80 ms/s SAR ADC using binary weighted split DAC with a Merged Capacitor Switching technique (MCS). The MCS technique used in the split capacitor arrays reduces the required number of unit capacitors by 50% as compared with the conventional ones [10]. The proposed technique effectively enhances the speed, the

power consumption, and the chip area of the ADC. Also, the presented ADC includes a comparator with offset cancellation and uses digital calibration for error correction. DNL and INL of this ADC are less than 0.37dB and 0.40 dB respectively and it shows a SFDR and SNDR of 66.72 dB and 50.71 dB respectively. In 2010, U-Fat Chio et. al proposed a new architectural concept that uses a 5-bit flash as the first stage and 5-bit SAR as the second stage with digital error correction that brings the resolution in 9-bit [11]. The solution doubles the optimal speed of operation of SAR ADCs at the relative low power cost of a low resolution results.

In 2011, Mehdi Saberi et. al presented a closed form formulas for the power consumption as well as standard deviation of INL and DNL for three commonly used architectures i.e. conventional binary weighted capacitive array, binary weighted capacitive array with attenuation capacitor and split binary weighted capacitor array including the effect of parasitic capacitances [12]. The proposed equations provide closed-form relations between the power consumption of the DAC as well as its INL and DNL metrics versus the size of the unit capacitor, the converter resolution, the clock frequency and the reference voltage. In 2012 HYEOK-KI HONG et. al designed a 7bit 1GS/s 7.2mw non-binary 2b/cycle SAR ADC that uses a non-binary decision scheme for decision error correction in a 2b/cycle structure not only increases the ADC speed with a relaxed DAC settling requirement [13].

In 2013, Yan Zhu et. el presented a SAR ADC with split DAC structure based on conventional charge redistribution and VCM based switching method and analyzed INL, DNL and the parasitic effects of the split DAC. Internal node parasitic in the split DAC degrades the conversion linearity and thus code randomized calibration technique was proposed to reduce the conversion non-linearity. Even after calibration of conventional switching method, V_{CM} based split DAC structure provided superior conversion linearity [2]. DNL and INL of the conventional switching method are +0.9/-0.7 LSB and +1/-1.1 LSB after calibration respectively and of V_{CM} based switching are +0.79/-0.27 LSB and +0.86/-0.78 LSB. Arindam Sanyal et. al proposed a high energy efficient capacitor switching scheme for SAR ADC [14] that achieves a zero energy dissipation in the first 2 comparison cycles and 4 times reduction in total capacitance used in the digital to analog converter. Hua Huang et. al presented a 6-GS/s 6-bit time-interleaved successive approximation register (SAR) analog to digital converter (ADC) [15]. The ADC consists of 32 single SAR-ADCs. The measured effective-number-of-bits (ENOB) at sampling rate of 6.144 GS/s are 5-bit at DC and 3.6- bit at the Nyquist frequency. The power consumption of the ADC-core without I/O's and 4-to-1 output MUX is 359 mW for an input swing of 1 V peak to peak differential, resulting in a FOM of 4.9 pJ/conv**.**

In 2014, Jiayi Hin et. al proposed an energy efficient SAR ADC for ultra low power applications by using asynchronous 2 bit/step scheme with a Hybrid R-2R/C-3C that halves both the conversion time and DAC switching activities and hence reduces the static and dynamic energy consumption [16]. Seon-Kyoo Lee et.al presented a 100 KS/s, 1.3µW, 9.3 ENOB SAR ADC with time domain comparator that utilizes a differential multi-stage Voltage Controlled Delay Lines [17] ,resulting in a highly digital operation eliminating static power consumption. Hung-Yan Tai et. al presented a 6-bit 1-GS/s single-channel two-step successive approximation register (SAR) analog-to-digital converter (ADC) using a source follower as an interstage residue amplifier. An asynchronous SAR ADC with two-step timing can effectively

allocate the bit-resolving procedure into the whole clock period and eliminate a dedicated duty-cycle clock generator [18]. The arbitrary weight capacitor array technique is utilized to tolerate offset mismatch between the coarse and fine stages. The level-shift technique is used to accelerate the comparator. It consumes 5.3mW at 1 GS/s and achieves a figure of merit of 180 fJ/conversion step.

Arindam Sanyal and Nan Sun presented a highly energy-efficient switching scheme for successive approximation register (SAR) analog to digital converters that achieves a 95% reduction in switching energy over the conventional SAR [19]. The switching energy has been calculated by taking into account both the power drawn from reference and the power consumed by the switches themselves. The frequency dependence of the switching energy has been studied and the proposed technique presents ways to maintain high energy efficiency over the entire frequency range of operation.

Younghoon Kim and Changsik Yoo presented a 100-kS/s time-domain analog-to-digital converter (TDADC) with successive approximation register architecture provides 8.3 effective bits. The time-domain comparator of the TDADC is realized with only one delay line consisting of a digitally controlled delay line and a voltage-controlled delay line [17]. Therefore, the linearity degradation due to the mismatch between multiple delay lines can be avoided.

III. Summary

Although various capacitive DAC based SAR registers have been designed which provide better results, they are making the simplest structure of SAR a complex one by increasing the complexity of SA control logic, comparator, DAC capacitive array which further reduces the resolution even at low speed. Errors mentioned still exist even with reduced values with the previously designed SAR's. So still there is a need to design a Successive Approximation Register Analog to Digital converter which is simplest, provides high resolution and consume low power with accurate results. Yan Zhu et. al presented a V_{CM} based switching approach for split SAR ADC that it further needed a code randomized calibration technique to improve it .Hung-Yen Tai et. al presented a 2b/step SAR ADC with 1GS/s sampling speed but with a very low resolution i.e. only 6-bit.Jiani Jin et. al presented a Hybrid R-2R/C-3C DAC structure for SAR ADC but it provided a very low sampling speed i.e. only 100KS/s. Hua Huang et. al presented a 6 GS/s Time Interleaved SAR ADC based on charge redistribution DAC but with a resolution of 6-bits.Younghoon Kim et. al presented a SAR ADC based on time domain comparator with supply voltage of 0.6V, but it resulted in a sampling speed of 100KS/s [17]. Table No. I summarizes the ADC performance and shows the comparison with the recently published ADCs.

TABLE 1 (Comparison Summary)

Architecture	[5]	[6]	[7]	[8]	[10]	[11]	[13]	[15]	[16]	[17]	[18]	[19]
Technology	90nm	90nm	0.13µm	0.13µm	65nm	90nm	45nm	90nm	180nm	0.18µm	40nm	0.11µm
Resolution (bit)	10	8	10	6	9	9	7	6	10	10	6	
Sampling Rate (MS/s)	100	180	50	1250	80	90	1000	6000	100	100K	1000	100K
Supply Voltage (V)	1.2	1.2	1.2	1.2	1	0.9	1.25		0.6	0.6	1.2	0.6
SNDR (dB)	56.6	48	52.8		66.72	51.8	40.8	32 (w calibration) 20 (w/o calibration		57.7	31.2	
ENOB (bit)	9.1		8.48	5.8 @ 1250MS/s 5.5 @ 1000MS/s			>6	5bit @DC 3.6bit @ 3.6GH	9.2	9.3	5.6	8.02
DNL (LSB)	0.79/-0.27				±0.37	0.87/-0.81	0.4/-0.4		0.5/-0.26	0.4/-0.7	0.59/-0.65	0.71/-0.84
INL (LSB)	0.86/-0.78				±0.40	0.71/-1.55	0.5/-0.2	1.1	0.89/-0.82	0.8/-0.7	0.58/-0.65	0.47/-0.91
FOM fJ/CS	55		52		39 (w/o reference) 38 (w reference)	472	80	4.9	6.7	21	180	65
Power (mW)	3	4	0.92	=32	1.7 (w/o reference) 3.4 (w reference)	13.5nW	7.2	0.36 (w core) 0.78 (w chip)	390 nW	1.3 µW	5.3	1.7 µW

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